The development and implementation of a hands-on, multidisciplinary product development course series at Georgia Tech

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ABSTRACT: A multidisciplinary, two-semester, Design-Build-Operate (DBO) course sequence has recently been developed by the Packaging Research Center (PRC) at the Georgia Institute of Technology, Atlanta, USA. This programme enables undergraduate and first-year graduate students to gain hands-on experience in design, fabrication processes, material systems, electrical testing, flip-chip assembly, thermal management and reliability assessment. The first course, *Electronic Packaging Substrate Fabrication* (DBO1), covers the fundamentals of the substrate fabrication processes and is augmented by interactive multimedia courseware that allows remote access through the Internet. The second course, *Package Assembly, Reliability, and Thermal Management* (DBO2), consists of electronics assembly processes, material systems, testing, thermal management and reliability assessment. The unique feature of the DBO course sequence is that it encompasses electrical engineering, mechanical engineering, chemical engineering and materials science and engineering concepts. The article reviews the methodology and infrastructure that was created to make the DBO course sequence a reality. The article also describes results based on student successes during each step of the fabrication process.

INTRODUCTION

One of the primary missions of engineering institutions is to produce graduates who can be gainfully employed by industry. For this to take place in today's industrial environment, it is imperative that graduates not only are armed with the latest theoretical knowledge in the field, but also with hands-on skills [1][2]. Due to its multidisciplinary nature, microelectronics packaging education offers significant challenges that have not been generally faced by academics dealing with curricula in the classical disciplines in engineering. A successful curriculum in packaging has to draw upon the subject matter in the disciplines of mechanical, electrical, chemical and materials engineering.

In response to these needs, the Packaging Research Center (PRC) at the Georgia Institute of Technology, Atlanta, USA, in partnership with the US electronics industry, has embarked upon a comprehensive, system-level and global electronic packaging education programme [3][4]. The PRC's education goals target students at all levels, particularly focusing on undergraduate education reform as a core strategy. In order to develop a successful undergraduate programme, the PRC has identified the following required elements:

- Fundamental and system-level classroom courses with an emphasis on theory;
- Availability of state-of-the-art laboratory facilities and hands-on system-level courses;
- Team-oriented research;
- Mechanisms for the inclusion of an industrial perspective;
- The development of an undergraduate textbook.

The PRC has focused on all of these elements and developed special programmes to address each. This article discusses the development and implementation of a new course sequence that provides students with hands-on experience.

BACKGROUND

Traditionally, institutions of higher learning have only taken research to the point of invention and, in some cases, to technical feasibility. Similarly, few research universities have ventured into the realm of developing system-level prototypes, which has traditionally been the sole responsibility of private industry. While universities have concentrated on new concepts, explored technologies and published journal papers, companies have performed their own exploration and subsequently focused on manufacturing. Therefore, there has been a major disconnect and, to a large degree, the novel concepts of universities have not reached the marketplace. The PRC was established to partner with industry to evolve this paradigm by taking research to the point of test beds.

The PRC hopes to balance the above deficiencies by taking a unique approach: Design-Build-Operate (DBO) research and education. This approach involves two fronts: research advances to develop next-generation system-on-a-package (SOP) architectures; and educating multidisciplinary teams of students, both graduate and undergraduate, in system-level, next-generation prototypes, from concept to design to development to test to operation. SOP integrates not only the digital functions, but also analogue, RF, optical and MEMS functions [5]. SOP technology promises to be lower in cost, higher in electrical system-level performance and faster to market, without the legal issues associated with system-on-a-chip (SOC) approaches [6]. A cross-section of the proposed SOP is shown in Figure 1. The DBO courses cover elements of SOP fabrication, assembly, testing and reliability assessment.

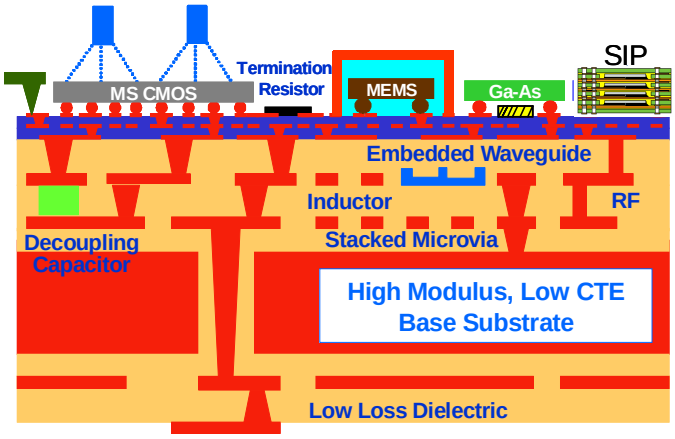

Figure 1: Georgia Tech's PRC system-on-a-package concept.

The DBO programme involves a hands-on course on next-generation substrate fabrication, *Electronic Packaging Substrate Fabrication* (DBO1), which includes electrical design, fabrication of conductors, dielectric, resistors, capacitors, inductors and electrical testing of these components. The subsequent course, *Package Assembly, Reliability, and Thermal Management* (DBO2), focuses on next-generation module technology involving flip-chip assembly, functional test, reliability and thermal management. The entire programme is offered in two semesters. Approximately 30-40 students are involved on an annual basis. The first course is augmented by interactive multimedia courseware that makes the course material remotely accessible via the Internet.

ELECTRONICS PACKAGING SUBSTRATE FABRICATION COURSE (DBO1)

The DBO1 course is cross-listed in the Schools of Electrical and Computer Engineering, Chemical Engineering, and Materials Science and Engineering, and it also attracts students in the Schools of Mechanical Engineering, Industrial Engineering, and Chemistry. The prerequisites for the course are sophomore-level chemistry and physics. Each course introduces theoretical concepts in a single weekly lecture, which is supplemented by three hours of hands-on experience in weekly laboratory work. The course is worth three credit hours. Course material and the course handbook are also available on the Internet at:
www.ece.gatech.edu/research/labs/vc/packaging

The course lectures are tailored to the weekly laboratory experiments so that students understand the fundamentals behind the fabrication processes and characterisation of the fabricated components. The topics covered include:

- Introduction to electronics packaging;
- Laboratory safety;
- Electrical design and design tools;
- Dielectric/polymer deposition;
- Formation of microvias;
- Copper metallisation;
- Embedded passives;
- Solder mask fabrication;
- Substrate characterisation and testing.

The PRC staff, prior to the first offering of the course, designed the DBO1 test board. The features included in the design are 2, 4, 6 and 8 mil traces with daisy-chain vias, SMT footprints, patterns for inter-layer capacitance measurements and comb patterns for surface insulation resistance measurements. The minimum line width and via size used is 4 mils. A composite view of the design is shown in Figure 2. The board size is 6" x 6". The description of the contents of the course is provided in the following sections.

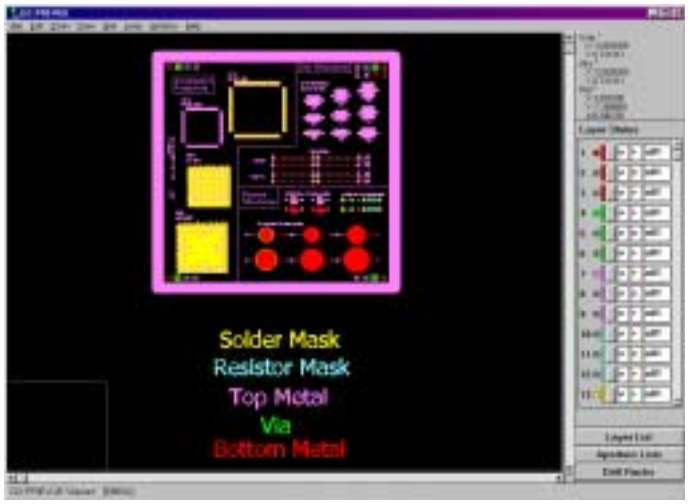

Figure 2: A composite layout of the 5-layer design.

Electrical Design

A design problem is given so that each student learns design rules and layout using the Cadence *Advanced Package Design* (*APD*) software. This package allows design on a per-layer basis and the definition of design rules that govern feature size and spacing. Students receive instruction on the meaning and function of these aspects of the software and gain experience in the layout of electrical design oriented towards manufacturability. Using this package, each metal and dielectric layer may be designed individually and may contain variable process and material parameters, including dielectric constant, loss tangent and layer thickness. *APD* may also be combined with electrical simulation tools in order to model specific design parameters prior to fabrication. Once the design is complete, *APD* creates industry-standard Gerber files that can be sent to generate photolithographic masks to be used in fabrication.

Fabrication Sequence

The process begins with surface preparation of the high-T_g, copper-clad, laminated FR-4 substrate and imaging the first layer using a conventional dry film photoresist, followed by printing and etching the first metal layer. The critical step is the application of the dry film dielectric polymer using spin coating, meniscus coating, or by conventional vacuum lamination. The metallisation of the second layer then takes places on the cured polymer using Pd catalysis and electroless copper deposition, followed by electroplating. The seed layer is then etched. A solder mask is applied to finish the board. There are two metal layers, but the total number of layers is five when the dielectric and solder mask layers are considered. The layers are: sub-etched metal 1, the dielectric layer, electroplated metal 2, the resistor layer and the soldermask. Fabrication is performed on both sides of the board, thus balancing each layer to minimise substrate warpage after each thermal cycle. Figure 3 depicts the complete 2-metal layer process sequence with an interlayer polymer dielectric film followed by resistor and soldermask layers.

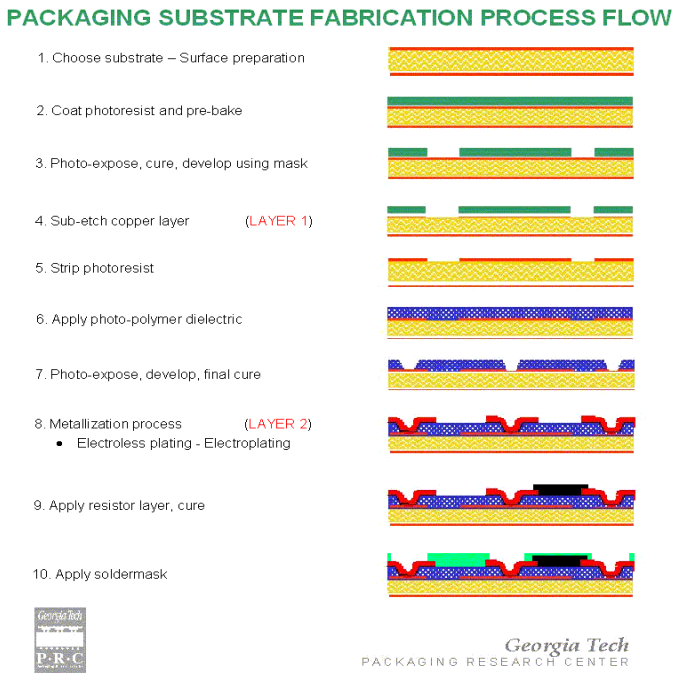

Figure 3: Process sequence for a 2-metal layer structure.

Substrate Characterisation and Electrical Test

Characterisation includes electrical tests for opens and shorts, capacitance measurements, and measurements of cross talk and impedance. Capacitance, resistance and inductance are measured using an LCR meter at 100 KHz. The measured resistance values are typically much higher than theoretical values computed based on sheet resistance, thickness, and width of the lines. The higher values are due to: incomplete filling and shrinkage of the polymer, resulting in a concave surface profile where the thickness at the centre is almost one-half that at the edges. Resistance values range from 15-75 kΩ for a continuous line with no breaks. The capacitance measurements show good agreement with theoretical values. Theoretical values are computed using the dielectric film thickness, dielectric constant of the epoxy film and the conductor area, as applicable, for the metal-insulated-metal (MIM) parallel plate capacitors. The experimental capacitance values range from 20-100 pF, depending on the electrode area, and the loss factor is approximately 0.02. For most boards, the yield for the inductors is approximately 50%. The Q-factor of the inductors varies from 5-10.

PACKAGE ASSEMBLY, RELIABILITY, AND THERMAL MANAGEMENT COURSE (DBO2)

This course focuses on hands-on experiences with electronic assembly processes, testing, thermal management, and reliability assessment. The course is cross-listed in the Schools of Electrical and Computer Engineering, Mechanical Engineering, and Materials Science and Engineering. The prerequisites for the course are sophomore-level chemistry and physics. Similar to DBO1, the format of the DBO2 course is one-hour weekly lectures, supplemented by four hours of hands-on experience in weekly laboratory work. The course lectures cover the following topics: next-generation packaging; assembly processes and materials; thermo-mechanical modelling and reliability; functional testing; thermal management; and reliability testing. The laboratory is equipped with state-of-the-art equipment.

Flip Chip Assembly Experiments

Surface Mount Technology (SMT) and flip assembly processes are taught to students through practical demonstrations. Students begin learning the SMT process by selecting a substrate (FR-4), components (PBGA and QFP) and lead-free solder paste. They are taught to program a screen printer and align the substrate under its stencil. After printing the solder paste on the component pads, students proceed to assemble the PBGA and QFP on the substrate. X-ray inspection is used to detect assembly offset. The assembled board is then reflowed in a BTU oven that uses standard eutectic solder. After reflow, the boards are inspected for voids and cracks using a Sonoscan system and x-ray. The students proceed by selecting flip chips (FA10, PB8, FB500), rosin, mild activated flux, underfill, and a pick-and-place machine. The pick-and-place machine is pre-programmed to place the chips on the substrate. Students dispense flux on the substrate (on the sites of the flip chips) and use the placement machine to assemble the chips. The assembly is inspected for possible misalignment using the X-ray system. After qualifying the assembly, the substrate is sent through the reflow oven once again. Next, students dispense underfill around the flip chips. The assembly is then sent through the reflow oven a final time and evaluated for flaws using the X-ray and Sonoscan systems. Using the above process, students conduct a wide range of experiments to investigate:

- Flip chips with no-flow underfill assembly;
- Flip chips with reworkable underfill assembly;
- Bump bond strength through a bump shear test;
- Solder paste, screen printing and SMT assembly;
- Die sectioning and electron microscopy;
- Electrical continuity, X-ray and Sonoscan tests;
- Reliability evaluation.

Underfill Materials Evaluation Experiments

Snap-cure underfill is the underfill material studied. The underfill is cured and sectioned into small pieces. One of the diced samples is placed in a thermo-gravimetric analyser (TGA) to study the decomposition of the material. A chart is drawn using the data and an estimate is made about the filler content in the underfill. Some underfill samples are used to study the CTE and *Tg* using a thermo-mechanical analyser (TMA). A dynamic mechanical analyser (DMA) is also used to study the loss modulus and the *Tg* of the underfill. Students then perform a flip chip assembly process for FA10 chips. An underfill volume study is implemented by selecting the snap-cure underfill and calculating the volume to be dispensed. An underfill dispenser is programmed and the calculated volume of underfill is dispensed. The assembly is then sent through a reflow oven and then evaluated for flaws using the Sonoscan Acoustic Microscope and X-ray systems.

Reliabilty and Moire Evaluation Experiments

After completing flip chip assembly, students conduct reliability evaluation. *ANSYS*, a finite element modelling software package, is presented as a means to model an FA10 flip chip. The program allows stress and strain data to be evaluated. A comparison is made between calculated and modelled values. A reliability test is conducted by each student by subjecting an FPGA assembly to air thermal cycling (-55 - 125 °C). After 100 thermal cycles, the FBGA is sectioned and polished, and a grating is transferred to

the polished surface through a standard process. After baking the samples, students use the Moire technique to study *u* and *v* displacements in the assembly. Using a standard software package, they calculate the stress and map it onto the captured Moire pattern.

Thermal Management Experiments

Students are taught thermal management by experimenting with different methods of cooling a high-power chip. They are given several types of heat sinks and their thermal resistance is calculated and evaluated for heat dissipation. The experiments are extended to study new technologies in forced convection versus natural convection by using cooling fans for natural cooling and synthetic microjects for forced cooling.

Electrical Test Experiments

A module is also fabricated to evaluate high speed testing strategies. The electrical test module is shown in Figure 4. The students learn how to use an HP 830000-F660 high-speed tester to conduct tests using a field programable gate array at 660 MHz, with 1.6 ns cycle time. They also learn about concepts like built-in-self-test (BIST).

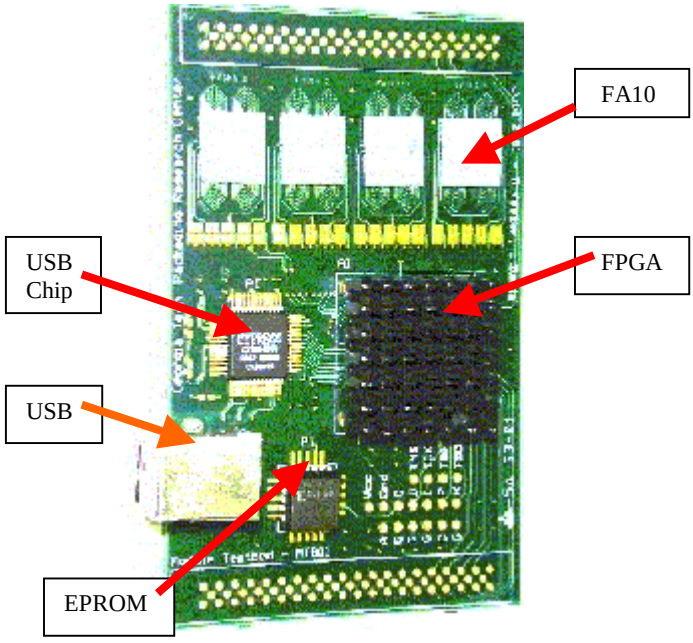

Figure 4: DBO2 electrical test module.

ASSESSMENT

Since its first offering in the fall of 1999, each DBO course has attracted 15-24 students per semester. Depending on the number of registrants, either two or three laboratory sessions were offered every week with no more than eight students per session. The students have evaluated the courses and instructors on an ongoing basis and they have generally been very positive about their learning experience. Some of the key student feedback extracted from these surveys is as follows:

- The availability of next-generation equipment and the hands-on experience better preprared students for industry.
- The multidisciplinary content of the course, with topics ranging from design to fabrication, provided solid knowledge in electronic packaging.
- The course promoted teamwork: students from electrical, chemical and mechanical engineering worked together to identify problems and solutions.

Students who completed these two courses gathered practical experience in substrate processing and assembly of microsystems. These courses are offered at the undergraduate level using a state-of-the-art facility, which is a unique contribution of the Georgia Tech PRC to the international packaging community and packaging education.

CONCLUSIONS

A unique, two-course Design-Build-Operate (DBO) sequence has been developed by the Packaging Research Center at Georgia Tech. The course on electronics pakaging substrate fabrication (DBO1) teaches substrate processing technology in a production-like environment. Students who complete this course and the subsequent course on assembly, reliability and thermal management (DBO2) gather practical experience in substrate processing and assembly of microsystems. A salient feature is that these courses are offered at the undergraduate level using a state-of-the-art facility.

Faculty members appreciate the benefits of a hands-on course sequence that allows students to directly observe the fabrication of a substrate, as opposed to trying to visualise sequential build-up processes. Students benefit from their exposure to a clean room environment, which requires them to follow standard protocol for such a facility and learn the importance of safe laboratory practices. This experience is invaluable to students seeking jobs or future research experiences requiring the use of such facilities. Finally, the exposure of students to practical, as well as theoretical, knowledge is a great benefit to industry employers. This experience has proven to be an important asset to students seeking co-op or intern positions. Students are able to *hit the ground running* when they accept employment.

ACKNOWLEDGEMENTS

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